NTMD2C02R2

Preferred Device

Power MOSFET 2 Amps, 20 Volts

Complementary SOIC−8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain−to−source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc−dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

Features

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive − Can Be Driven by Logic ICs
- Miniature SOIC−8 Surface Mount Package − Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SOIC−8 Package Provided
- Pb−Free Packages are Available

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) (Note 1)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage N−Channel P−Channel	V_{DSS}	 20 20	Vdc
Gate−to−Source Voltage	V_{GS}	±12	Vdc
Drain Current − Continuous N−Channel P−Channel − Pulsed N−Channel P−Channel	I_D I_{DM}	5.2 3.4 48 17	A
Operating and Storage Temperature Range	T_J and T_{stg}	−55 to 150	°C
Total Power Dissipation @ T_A= 25°C (Note 2)	P_D	2.0	W
Thermal Resistance − Junction to Ambient (Note 2)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds.	T_L	260	°C

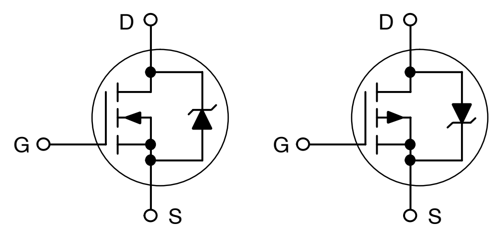
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Negative signs for P−Channel device omitted for clarity.
2. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

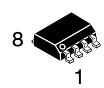
ON Semiconductor®

http://onsemi.com

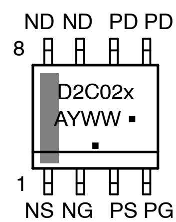
2 AMPERES
20 VOLTS
$R_{DS(on)}$ = 43 mΩ (N−Channel)
$R_{DS(on)}$ = 120 mΩ (P−Channel)



MARKING DIAGRAM & PIN ASSIGNMENT



SOIC−8
CASE 751
STYLE 14



D2C02	=	Specific Device Code
x	=	Blank or S
A	=	Assembly Location
Y	=	Year
WW	=	Work Week
▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMD2C02R2	SOIC−8	2500/Tape & Reel
NTMD2C02R2G	SOIC−8 (Pb−Free)	2500/Tape & Reel
NTMD2C02R2SG	SOIC−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Note 3)

Characteristic	Symbol	Polarity	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)	$V_{(BR)DSS}$	(N) (P)	20 20	– –	– –	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = 20 Vdc) (V_{GS} = 0 Vdc, V_{DS} = 12 Vdc)	I_{DSS}	 (N) (P)	 – –	 – –	 1.0 1.0	μAdc
Gate−Body Leakage Current (V_{GS} = ±12 Vdc, V_{DS} = 0)	I_{GSS}	–	–	–	100	nAdc
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	(N) (P)	0.6 0.6	0.9 0.9	1.2 1.2	Vdc
Drain−to−Source On−Resistance (V_{GS} = 4.5 Vdc, I_D = 4.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 2.4 Adc)	$R_{DS(on)}$	 (N) (P)	 – 0.07	 0.028 –	 0.043 0.1	Ω
Drain−to−Source On−Resistance (V_{GS} = 2.7 Vdc, I_D = 2.0 Adc) (V_{GS} = 2.7 Vdc, I_D = 1.2 Adc)	$R_{DS(on)}$	 (N) (P)	 – 0.1	 0.033 –	 0.048 0.13	Ω
Forward Transconductance (V_{DS} = 2.5 Vdc, I_D = 2.0 Adc) (V_{DS} = 2.5 Vdc, I_D = 1.0 Adc)	g_{FS}	 (N) (P)	 3.0 3.0	 6.0 4.75	 – –	Mhos

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Polarity	Min	Typ	Max	Unit
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	(N) (P)	– –	785 540	1100 750	pF
Output Capacitance		C_{oss}	(N) (P)	– –	210 215	450 325	
Transfer Capacitance		C_{rss}	(N) (P)	– –	75 100	180 175	

SWITCHING CHARACTERISTICS (Note 5)

Characteristic	Conditions	Symbol	Polarity	Min	Typ	Max	Unit
Turn−On Delay Time	(V_{DD} = 16 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω) (V_{DD} = 10 Vdc, I_D = 1.2 Adc, V_{GS} = 2.7 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	(N) (P)	– –	11 15	18 –	ns
Rise Time		t_r	(N) (P)	– –	35 40	65 –	
Turn−Off Delay Time		$t_{d(off)}$	(N) (P)	– –	45 35	75 –	
Fall Time		t_f	(N) (P)	– –	60 35	110 –	
Turn−On Delay Time	(V_{DS} = 16 Vdc, I_D = 6.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω) (V_{DS} = 10 Vdc, I_D = 2.4 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	(N) (P)	– –	12 10	20 20	
Rise Time		t_r	(N) (P)	– –	50 35	90 65	
Turn−Off Delay Time		$t_{d(off)}$	(N) (P)	– –	45 33	75 60	
Fall Time		t_f	(N) (P)	– –	80 29	130 55	
Total Gate Charge	(V_{DS} = 10 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc) (V_{DS} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc)	Q_T	(N) (P)	– –	12 10	20 18	nC
Gate−Source Charge		Q_1	(N) (P)	– –	1.5 1.5	– –	
Gate−Drain Charge		Q_2	(N) (P)	– –	4.0 5.0	– –	
		Q_3	(N) (P)	– –	3.0 3.0	– –	

3. Negative signs for P−Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

ELECTRICAL CHARACTERISTICS – continued (T_A = 25°C unless otherwise noted) (Note 6)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
SOURCE−DRAIN DIODE CHARACTERISTICS (T_C = 25°C)							
Forward Voltage (Note 7)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.4 Adc, V_{GS} = 0 Vdc)	V_{SD}	(N) (P)	– –	0.83 0.88	1.1 1.0	Vdc
Reverse Recovery Time	(I_F = I_S, dI_S/dt = 100 A/μs)	t_{rr}	(N) (P)	– –	30 37	– –	ns
		t_a	(N) (P)	– –	15 16	– –	
		t_b	(N) (P)	– –	15 21	– –	
Reverse Recovery Stored Charge		Q_{RR}	(N) (P)	– –	0.02 0.025	– –	μC

6. Negative signs for P−Channel device omitted for clarity.
7. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

N−Channel

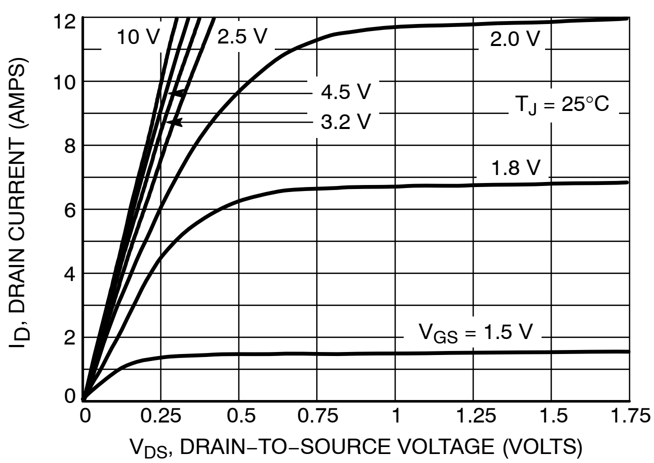


Figure 1. On−Region Characteristics

P−Channel

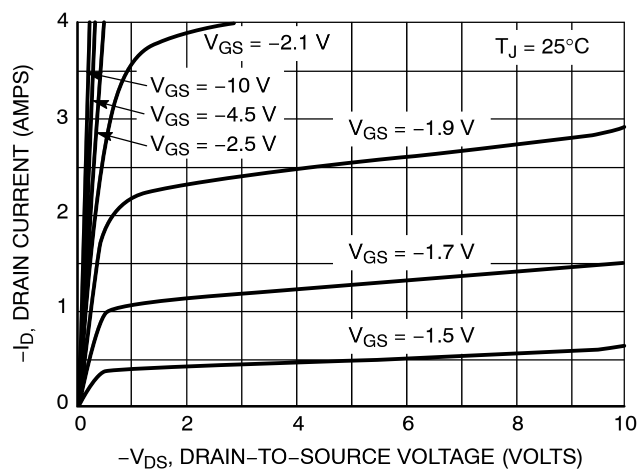


Figure 2. On−Region Characteristics

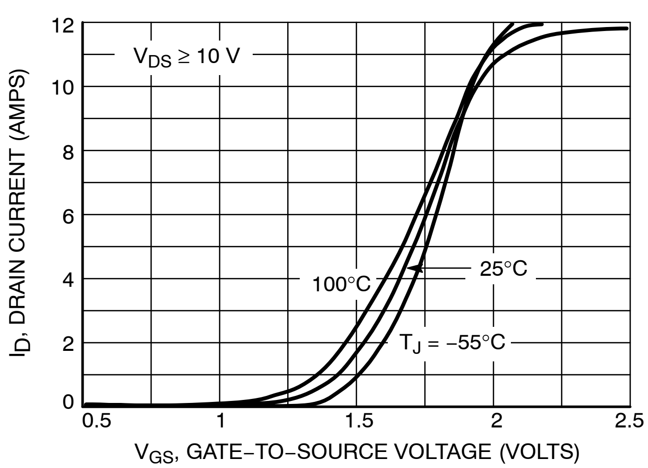


Figure 3. Transfer Characteristics

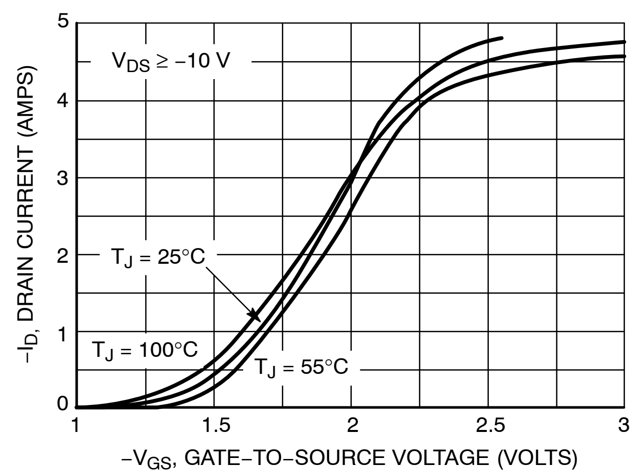


Figure 4. Transfer Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS

N−Channel

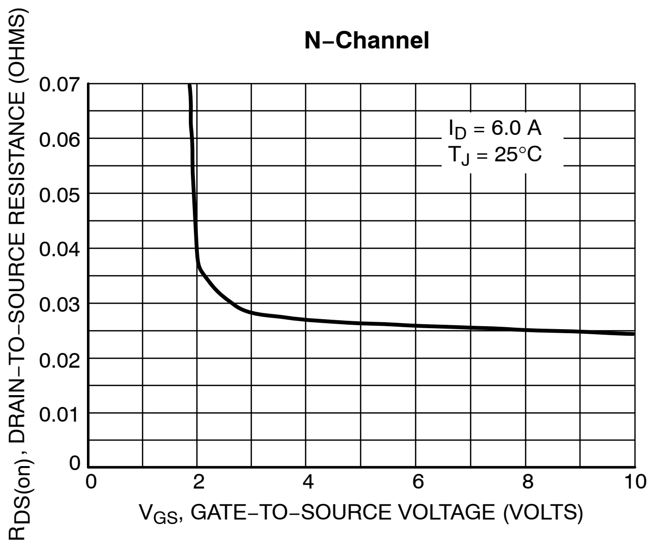


Figure 5. On−Resistance versus Gate−To−Source Voltage

P−Channel

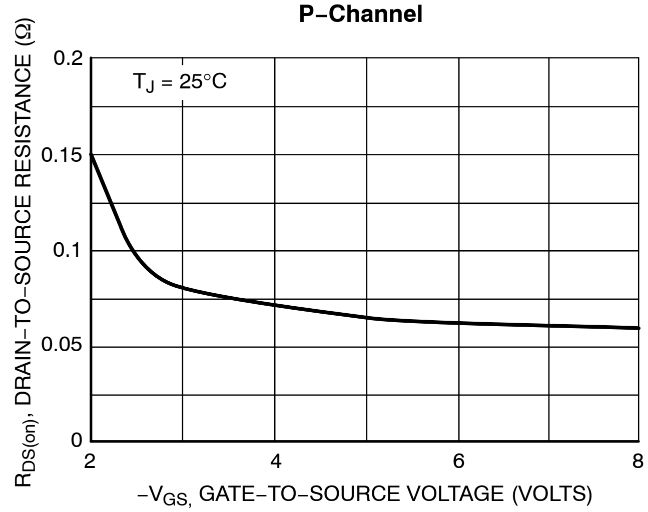


Figure 6. On−Resistance versus Gate−To−Source Voltage

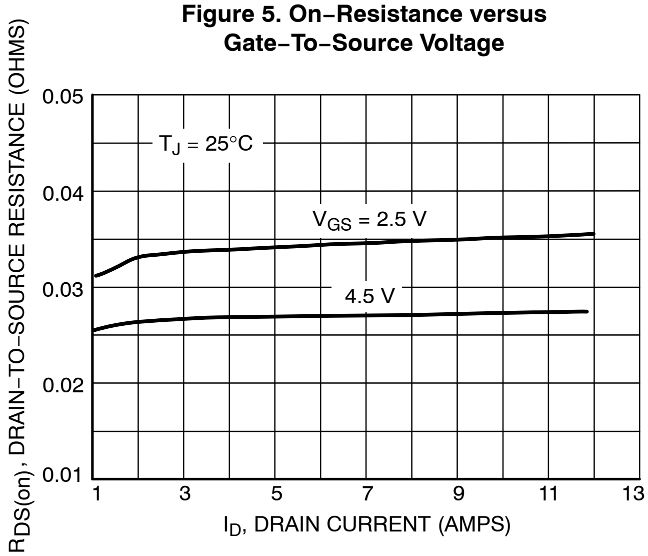


Figure 7. On−Resistance versus Drain Current and Gate Voltage

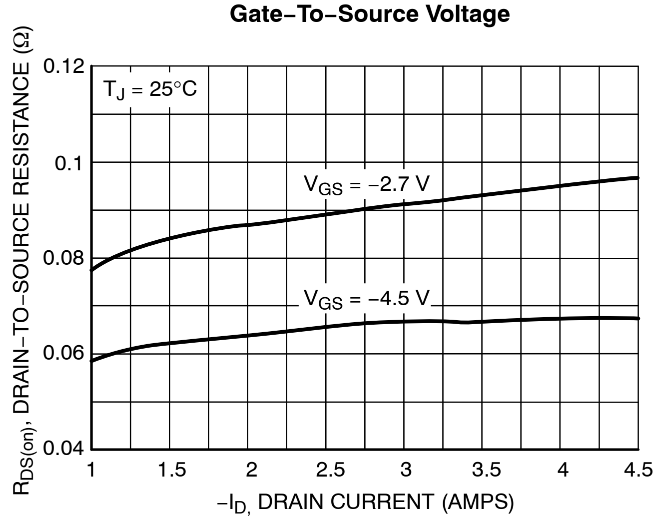


Figure 8. On−Resistance versus Drain Current and Gate Voltage

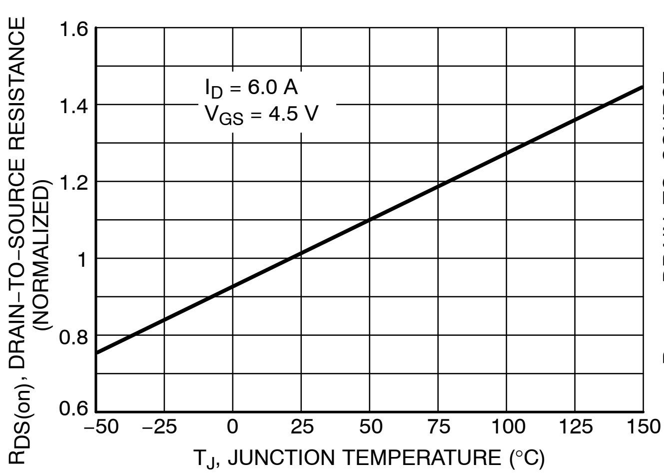


Figure 9. On−Resistance Variation with Temperature

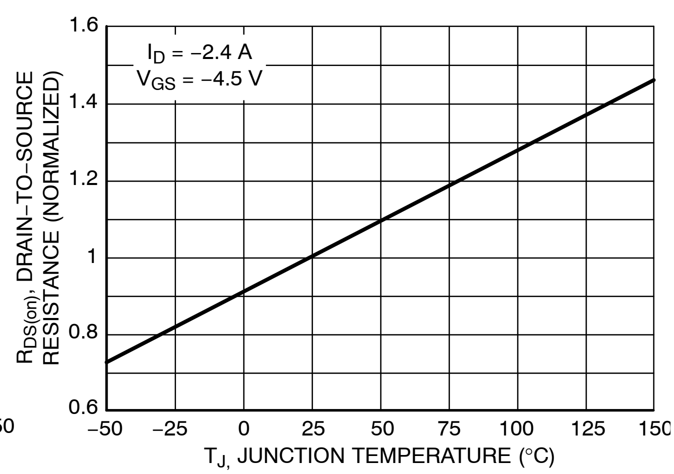


Figure 10. On−Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

N−Channel

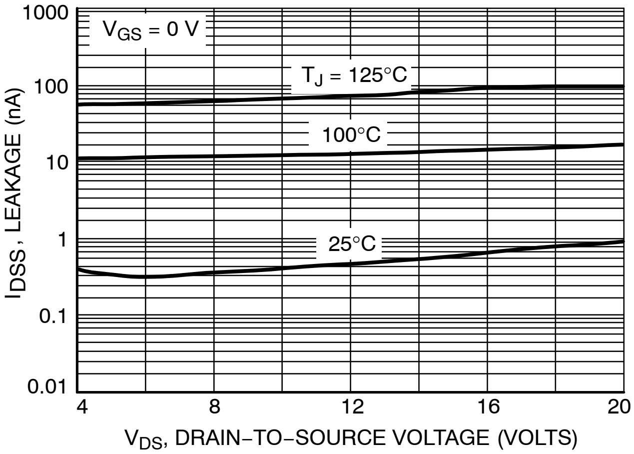


Figure 11. Drain−To−Source Leakage Current versus Voltage

P−Channel

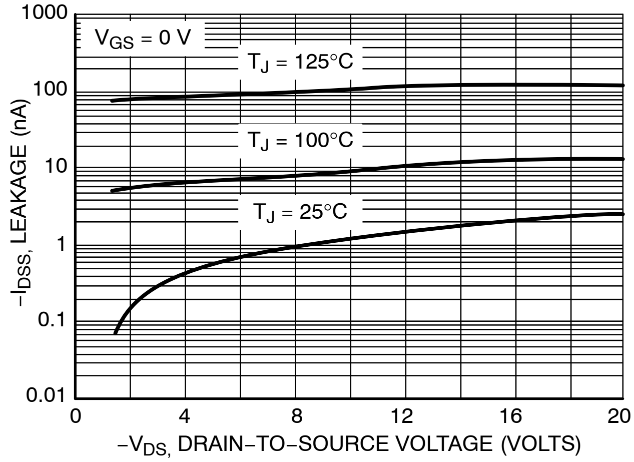


Figure 12. Drain−To−Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain−gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn−on and turn−off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off−state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on−state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figures 17 and 18) show how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figures is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

N−Channel **P−Channel**

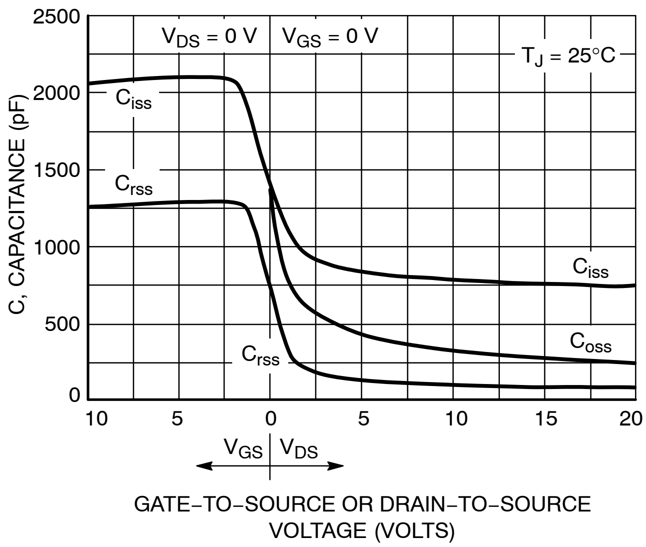


Figure 13. Capacitance Variation

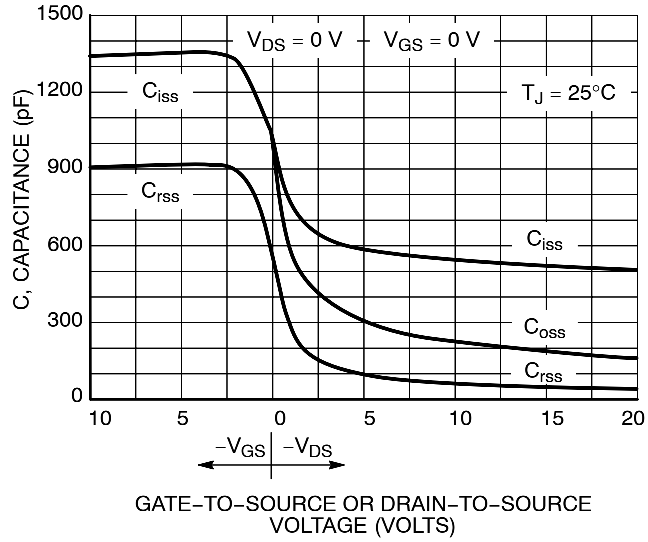


Figure 14. Capacitance Variation

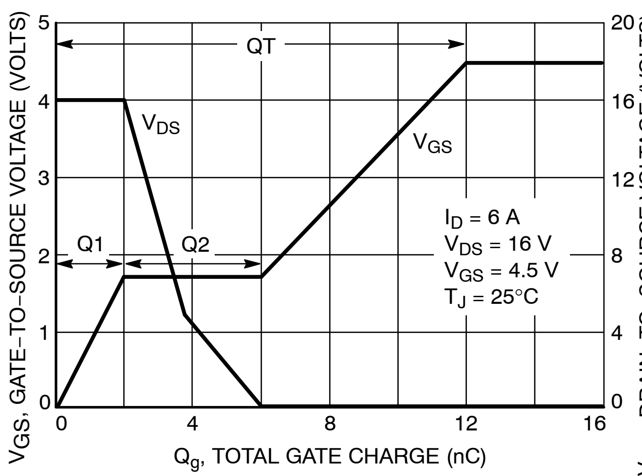


Figure 15. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

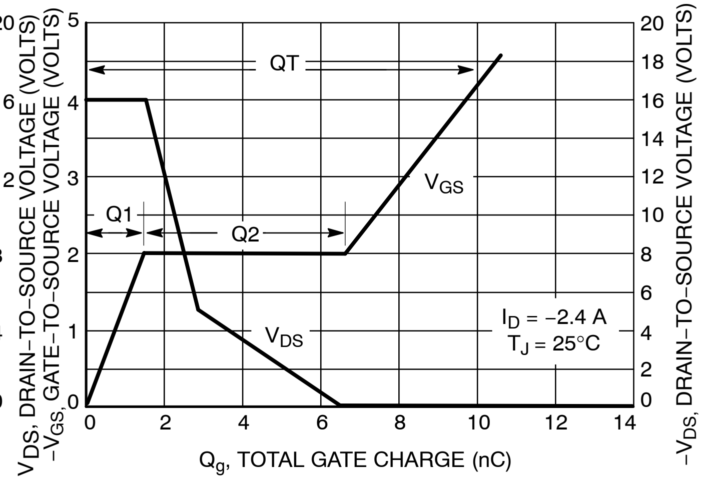


Figure 16. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

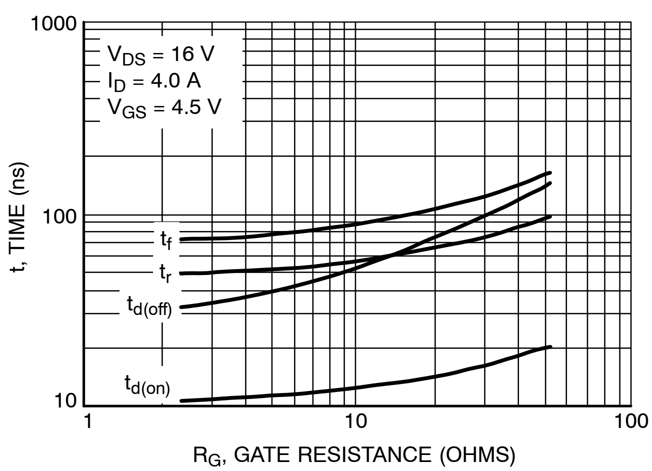


Figure 17. Resistive Switching Time Variation versus Gate Resistance

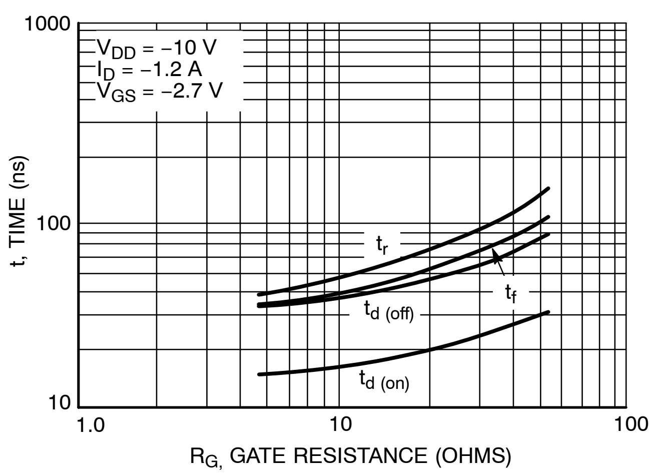


Figure 18. Resistive Switching Time Variation versus Gate Resistance

DRAIN−TO−SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 24. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

N−Channel

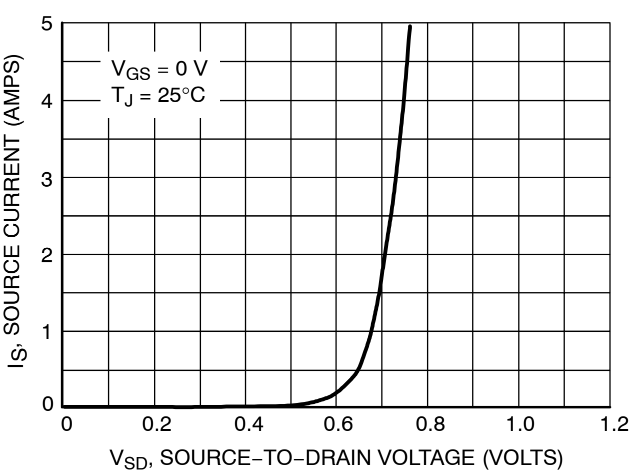


Figure 19. Diode Forward Voltage versus Current

P−Channel

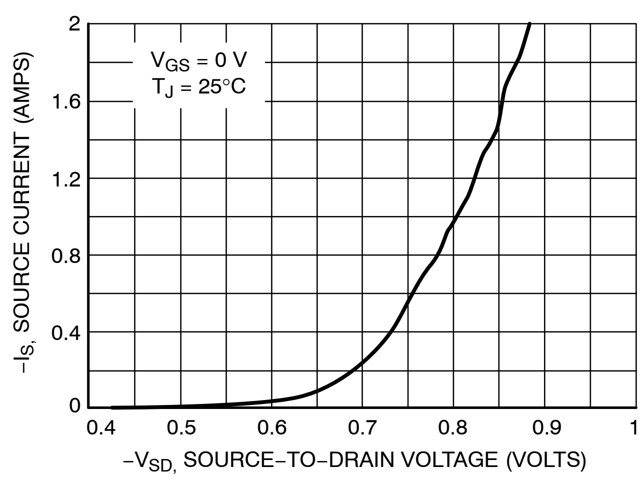


Figure 20. Diode Forward Voltage versus Current

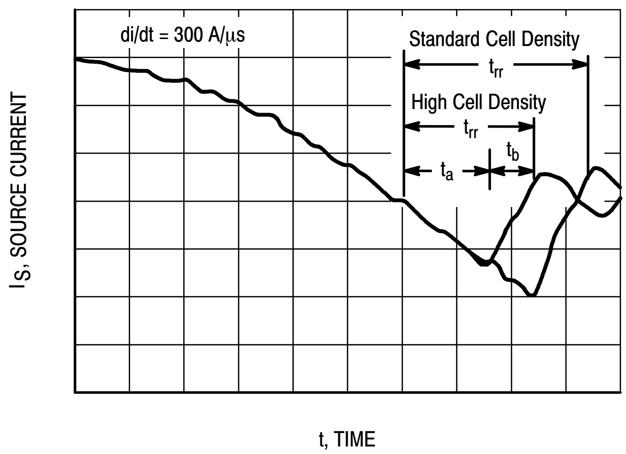


Figure 21. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance − General Data and Its Use."

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

N−Channel

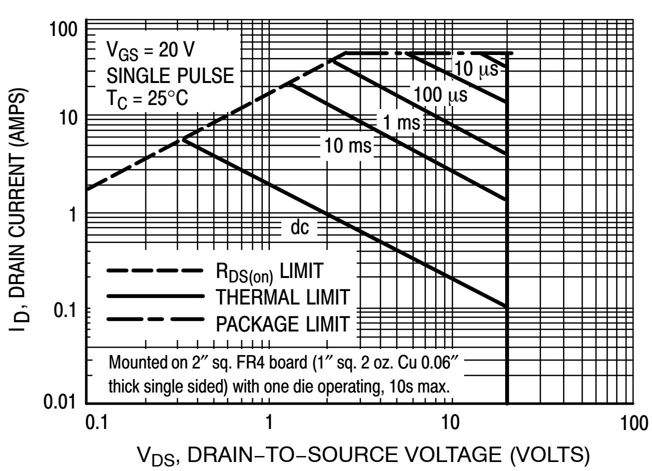


Figure 22. Maximum Rated Forward Biased Safe Operating Area

P−Channel

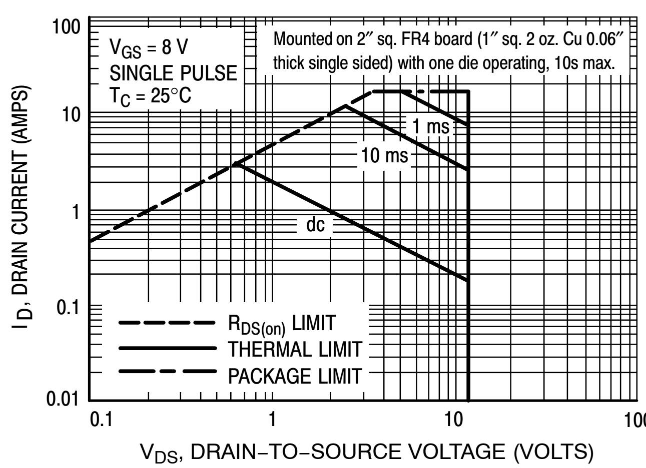


Figure 23. Maximum Rated Forward Biased Safe Operating Area

TYPICAL ELECTRICAL CHARACTERISTICS

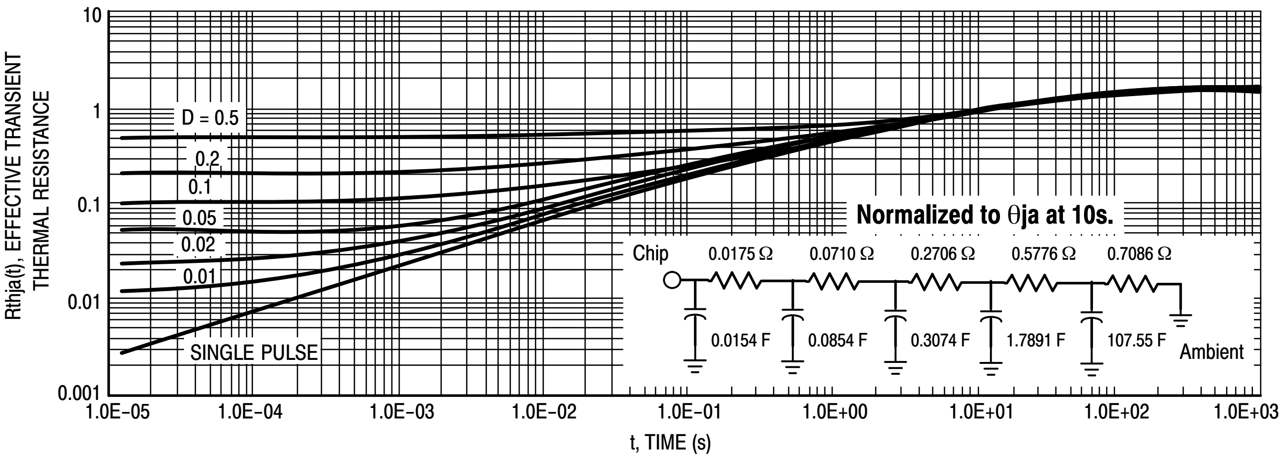


Figure 24. Thermal Response

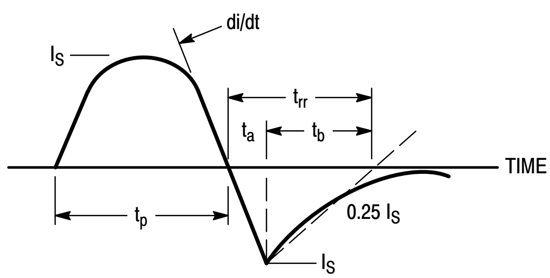
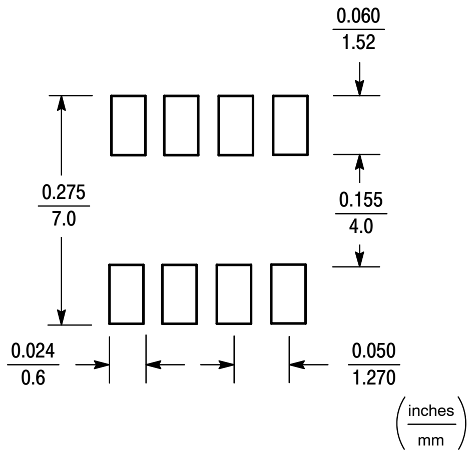


Figure 25. Diode Reverse Recovery Waveform

INFORMATION FOR USING THE SOIC−8 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self−align when subjected to a solder reflow process.



SOIC−8 POWER DISSIPATION

The power dissipation of the SOIC−8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, T_A. Using the values provided on the data sheet for the SOIC−8 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SOIC−8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad™, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

*Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 26 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177−189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

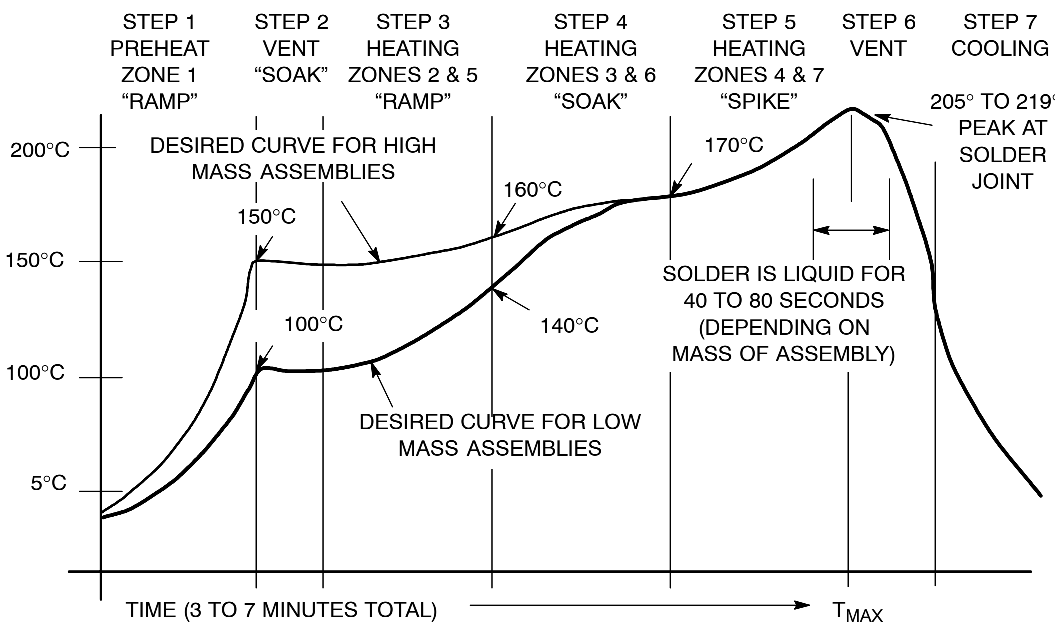
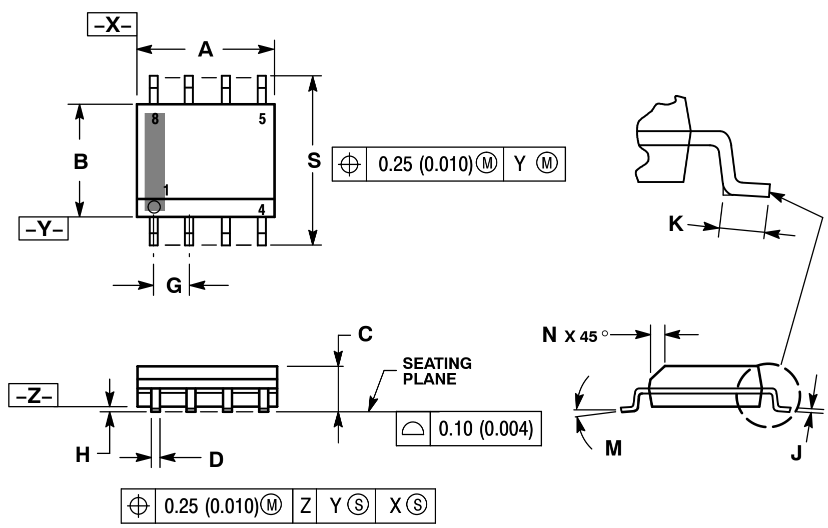


Figure 26. Typical Solder Heating Profile

PACKAGE DIMENSIONS

SOIC−8 NB
CASE 751−07
ISSUE AG

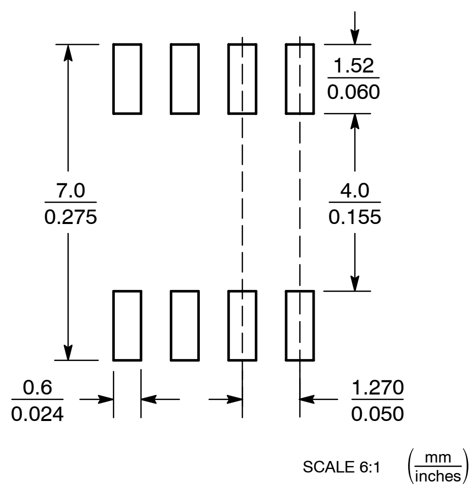


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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